Radiation Robustness Evaluation on XOR Logic Gates at 16nm CMOS and FinFET Technology

Rafael N. M. Oliveira and Cristina Meinhardt
Department of Informatics and Statistics, Federal University of Santa Catarina - UFSC
Florianópolis, Brazil
rafael.nmo@grad.ufsc.br, cristina.meinhardt@ufsc.br

***Abstract*—This work aims to compare a set of different transistors arrangements for XOR logic gates at 16nm considering two different technologies, Complementary Metal-Oxide Semiconductor (CMOS) and Fin Field-Effect Transistor (FinFET) and two different logic, Complementary Logic (CMOS logic) and Pass-Transistor Logic (PTL). The goal of this work is to identify how these two topologies behave in a specific environment analyzing the Linear Energy Transfer threshold for each one of them. This parameter allows designers to evaluate the robustness of the XOR cells against radiation faults. XOR gates based on PTL have shown robustness against radiation effects when compared with the XOR cells implemented with complementary CMOS logic. Further, FinFET-based circuits have shown to be about three times more robust than CMOS technology, with improvement for both logic families evaluated.**

***Index Terms*—XOR topologies, complementary CMOS, PTL, FinFET, LET, radiation effects**

I. Introduction

Technology scaling introduced new challenges in circuit design due to the tiny dimensions and process variability. Besides the dimension shrinking, the supply voltage is reduced to meet the design requirements such as reducing the consumption of dynamic power and also static power. In nanotechnologies, there is an increase of leakage currents featuring an increase in static consumption of logic gates [1].

Furthermore, the scaling process has a direct and negative impact on reliability [2]. At each new technology node, there is a significant increase in the number of possible faults, reflecting high device failure rates and low yield [3]. Advances in microelectronics have led the scale down of technology and reduction in the threshold voltage as well as the increase in operating frequencies. However, it causes an increase in the susceptibility of the circuit relative to the noise from the environment and particularly the bombardment of particles of radiation [4].

Even particles with low energy found on the surface of the Earth, previously overlooked, they are now able to interfere within the operation of the circuits [5]. Thus, one of the biggest challenges in the semiconductor industry is to ensure the reliability of circuits due to the interaction of ionizing particles in silicon.

For a long time, Single Event Transient (SET) was considered irrelevant due to the intrinsic capacity of the combinational cells to mask their effect. However, with each new generation of technology, the effects of masking have been reduced, increasing the need to study and develop SET mitigation techniques [6].

Complex arithmetic circuits and computer systems are composed by a set of logic gates. One of these cells is the exclusive-OR (XOR). Due to its large application, the electrical characteristics of XOR logic gates are very important because they should significantly affect the performance of these systems. Several works explore different implementations of an XOR gate, investigating new transistor arrangements, using new technologies, and observing the behavior of these circuits under critical situations, as for example low power operation, radiation environments or deep nanotechnology designs and their current challenges [7]–[15].

This work evaluates and compares these XOR gates using CMOS Logic and PTL, implemented with 16nm CMOS and FinFET technology. The main goal of this work is to provide electrical and behavioral information of XOR gates under fault tolerance.

II. Methodology

A set of nine different XOR topologies were chosen and the schematic diagram for each XOR gate is presented in Fig. 1. Four XOR implementations explore the conventional Complementary Logic family (V1-V4) [16] and five the PTL family (V5-V9). The Complementary Logic uses the concept of designing circuits from a complementary pull-up and pull-down network. It makes circuits present a better robustness against noise and reliable operation at low voltages when compared with PTL [17].

The PTL explores the use of transistors as switches to transmit logic levels between nodes of a circuit rather than switches connected directly to supply voltages. This enables the reduction of redundant transistors, leading many logic functions the capacity of achieving an implementation with a smaller area than complementary logic. However, their output signals tend to be more susceptible to noise.

The evaluation of the radiation robustness of the XOR gates is made under nominal supply voltage for CMOS and FinFET devices. Both technologies are simulated using the model provided by Arizona State University, through Predictive Transistor Model (PTM) at 16nm technology node [18]. The nominal supply voltage used was 0.7V for CMOS technology and 0.85V for FinFET technology.

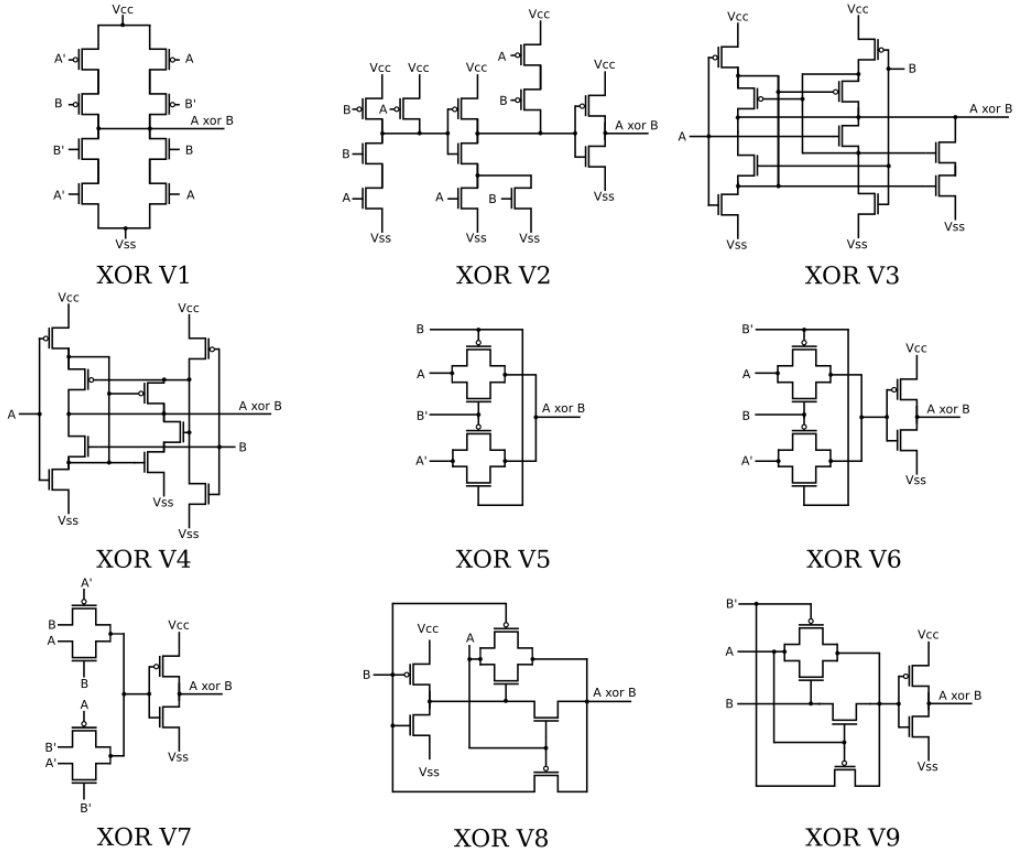

Fig. 1. XORs topologies explored in this work.

The impact that one ion causes in a junction depends on the amount of charge collected while it tracks into the depletion region, i.e. the Linear Energy Transfer (LET) [4]. The robustness of a cell is measured considering the LET threshold, i.e, the minimum energy that provokes an error in the system. The fault simulation of the ion hit at the junction of a device is carried out at the circuit level using HSPICE. The experiments consist in extracting minimum current that causes a fault on the device, based on an analytic solution [19]. To obtain the minimum current in a junction, the radiation effect is modeled as a double exponential transient pulse by inserting an independent current source at the sensitive node. For all topologies, the output node was the target of the fault injection because the output is always a sensitive node for XOR logic.

After that, the LET is calculated for all XOR gates using the Eq. (1). The Q_{coll}, defined by the Eq. (2)), is the amount of charge collected due to an ion strike in the junction. I_o is the minimum current to cause a fault, obtained by simulations. The term τ_α is the collection time constant of the junction and τ_β is the time constant for the initially establishing the track. For the devices used in this work, these constants are equal to 200ps for τ_α and 10ps for τ_β [20]. The term Q is the constant charge that the particle deposits along its track and L is the charge collection depth. The value for these constants are 10.8fC/μm and 2μm, respectively [21].

$$LET = \frac{Q_{coll}}{Q \times L} \tag{1}$$

$$Q_{coll} = I_o \times (\tau_\alpha - \tau_\beta) \tag{2}$$

For the CMOS technology, all transistors were sized based on the MOSIS CMOS scalable rules [22]. Each transistor has a channel length L = 16nm and channel width of NMOS transistor Wn = 32nm, and PMOS Wp = 64nm. For the FinFET technology, all transistors were sized based on design rules that explicitly demands a minimum sized of FinFET devices, with the number of fins equal to 3 and a channel length L = 16nm [23]. To analyze both logic families, two inverters were used as an input and four inverters (fanout-of-4) were used as a load in order to emulate a more realistic scenario [22].

This work consists of two steps: (I) logical validation of the arrangements and (II) data extraction: the minimum current to cause a fault in a junction, i.e. the LET threshold. The first step occurs when all XOR gates are implemented and its goal is to ensure the right behavior of the gate. The second step goal is to obtain all the maximum current values that produce logic upset, for all input combinations, and choose the worst case.

III. Results

The evaluation considers the electrical behavior of the circuits for CMOS and FinFET technologies, starting from the complementary logic XOR circuits then presenting the outcomes for the PTL XOR circuits. After that, a comparison between the logic families is discussed. The last comparison is made between both technologies. The average LET are summarized in Table I and all LET results in Table II.

TABLE I
AVERAGE LET VALUES ($keVcm^2/mg$)

Technology	CMOS logic	PT Logic	All XOR Versions
CMOS	16.71	21.64	19.45
FinFET	52.78	63.16	58.54

A. XOR CMOS Logic with CMOS

V2 was the most robust gate among the complementary CMOS topologies (V1-V4) with a LET of $27.27keVcm^2/mg$. It is twice greater than the other three gates (V1, V3, and V4), that had the same behavior with a LET of $13.19keVcm^2/mg$.

B. XOR PTL with CMOS

For the PTL topologies (V5-V9), V5 and V8 had the worst LET of $13.19keVcm^2/mg$. It is near 39% lower than the average of PTL topologies and up to 51% lower than the best cases (V6, V7, and V9).

C. CMOS technology: CMOS Logic and PTL comparison

Comparing complementary and PTL families it was noticed that the PTL topologies analyzed are more robust against radiation effects, with an average LET of $21.64keVcm^2/mg$ which is almost 30% greater than the average for complementary topologies ($16.71keVcm^2/mg$). Another point to notice is that V2, V6, V7, and V9 had better results for CMOS technology, as Fig. 2 shows, with a LET of $27.27keVcm^2/mg$.

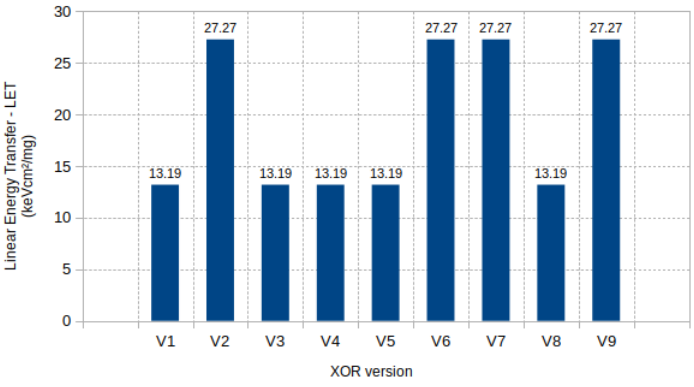

Fig. 2. LET worst cases for CMOS technology

D. XOR CMOS Logic with FinFET

For circuits with FinFET devices, from the CMOS logic topologies (V1-V4), V1 and V4 had the worst performance with a LET of $43.10keVcm^2/mg$, which is close to 18% lower than the average LET among the complementary topologies. Comparing these two topologies with the best case (V5) they have even worst results being almost 41% lower.

E. XOR PTL with FinFET

Among the PTL topologies, V8 had the worst LET of $43.10keVcm^2/mg$ which is up to 32% worst than the average . Comparing with the best case (V6, V7, and V9) topology V8 is even worst with its LET being close to 41% lower.

F. FinFET technology: CMOS Logic and PTL comparison

Comparing FinFET complementary and PTL topologies the same behavior noticed for CMOS technology of PTL topologies being more robust than complementary is replicated. The average LET for the PTL is up to 19% greater than the average for complementary logic. Topologies V2, V6, V7, and V9 presented the best LET results ($73.01keVcm^2/mg$), as showed in Fig. 3.

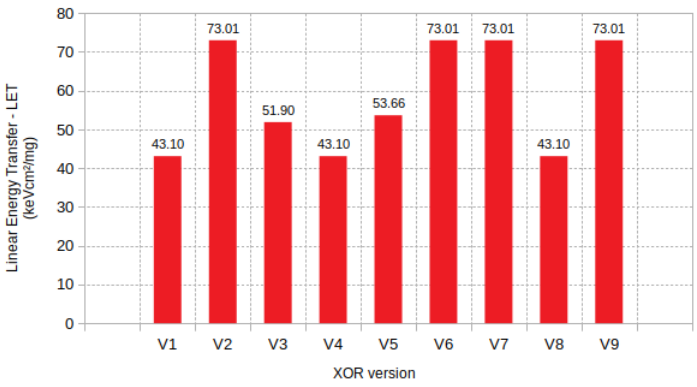

Fig. 3. LET worst cases for FinFET technology

G. CMOS and FinFET technology comparison

Finally, this work compares CMOS and FinFET circuits. The FinFET technology has performed an improved robustness compared to the CMOS technology at the two logic analyzed in this work. This can be explained by the better gate control over the channel. As shown in Fig. 4, the V2, V6, V7 and V9 gates have shown to be the most robust topologies in both technologies with LET = $27.27keVcm^2/mg$ for CMOS and LET = $73.01keVcm^2/mg$ for FinFET. XOR V1, one of the most common topologies found in standard cells, proved to be one of the most sensitive gate with a LET up to 25% lower than the average for both technologies. FinFET-based for PTL topologies have shown an average LET up to three times greater than CMOS-based devices and for complementary CMOS logic almost two times. Further, considering all topologies FinFET average LET has shown to be up to three times higher than CMOS-based devices.

IV. Conclusion

A comparative analysis of radiation sensitivity at different XOR logic gate topologies based on CMOS and FinFET devices are introduced in this paper. It was found that the topologies implemented with complementary CMOS logic

TABLE II
LET RESULTS ($keVcm^2/mg$)

	CMOS Logic					PTL			
Technology	V1	V2	V3	V4	V5	V6	V7	V8	V9
CMOS	13.19	27.27	13.19	13.19	13.19	27.27	27.27	13.19	27.27
FinFET	43.10	73.01	51.90	43.10	53.66	73.01	73.01	43.10	73.01

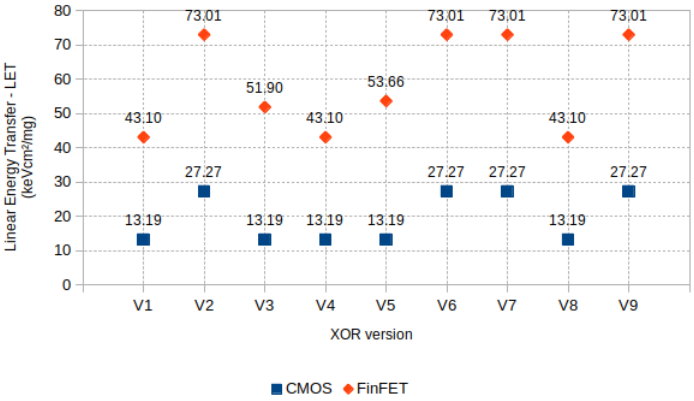

Fig. 4. LET worst cases for CMOS and FinFET technologies

might be more sensitive to radiation faults, at output node, than PTL topologies. For all analyzed circuits, FinFET circuits have shown to be more robust against radiation faults than the CMOS-based circuits. For both technologies, XOR V2, V6, V7, and V9 have shown to be the least sensitive to the radiation effects, considering both logic style. Also, circuits with FinFET devices improve robustness against faults, by average, more than two times for both complementary logic and PTL.

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